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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/508,865 | 02/08/2005 | Jean Surcaud | 0579-1069 | 8705 |

466 7590 08/22/2007

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| EXAMINER | |
|---|---|
| TRAIL, ALLYSON NEEL | |
| **ART UNIT** | **PAPER NUMBER** |
| 2876 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 08/22/2007 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/508,865 | SUREAUD, JEAN | |
| | Examiner | Art Unit | |
| | Allyson N. Trail | 2876 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-20* is/are rejected.

7)☒ Claim(s) *16-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Information Disclosure Statement*

2. The Information Disclosure Statement filed on September 24, 2004 has been considered. An initialed copy of the Form 1449 is enclosed herewith.

### *Claim Objections*

3. Claims 1-4, 7, 8, 10, 13, 15, and 17 are objected to because of the following informalities:

Re claims 1, 2, 4, 13, 15, and 17, line 2: replace "it" with --the electronic entity--.

Re claim 1, line 3: replace "its" with --the capacitive component's--.

Re claim 4, line 3: replace "it" with --the electronic entity--.

Re claim 7, line 3: replace "an" with --a--.

Re claim 8, line 2: either change the dependency from claim 7 to claim 6, or replace "said field-effect" with --a field-effect--.

Re claim 10: the phrase "is much greater" renders the claim indefinite because it is a relative term, which makes the limitation unclear.

Re claim 13, line 5: replace "their" with --the capacitive components'--.

Re claim 13, line 5: replace "it" with --the electronic entity--.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-6, 8, and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Berstis et al (2005/0185515), hereinafter Berstis.

With respect to claims 1 and 17-19, Berstis discloses in paragraph 0049 a transaction electronic entity (externally powered smart card). Berstis teaches in the abstract that the electronic entity includes capacitive component (insulated charge storage element, that receives an electrostatic charge through its insulating medium). Paragraph 0036 explains that the charge storage element leaks the electrostatic charge through its insulating medium through some type of physical process, thereby reducing the electric potential of the charge storage element. Paragraph 0039 goes on to explain that the capacitive component (insulated medium) passes a charge through the medium depending on the dielectric constant.

Paragraph 0049 discloses a means for coupling the capacitive component to an electrical power supply to be charged by the electrical power supply. "The programming unit may be physically coupled to a device containing the charge storage element during its programming operation, after which the programming unit is decoupled."

Paragraph 0043 explains that the programming unit 202 draws electrical power from electrical power supply A 204 for its operation. Paragraph 0035 also discloses a means for coupling the capacitive component to an electrical power supply to be charged by the electrical power supply. "In general, an insulated, charge storage element receives an amount of electrostatic charge through its insulating medium, i.e. the charge storage element is programmed, thereby giving the charge storage element a known electric potential with respect to points outside the insulating medium."

The electronic entity further includes a means for measuring the residual charge in the capacitive component. Paragraph 0049 discloses that at after decoupling from the charging supply, a time measurement unit may be physically coupled to the device containing the charge storage element (electronic entity) during its elapsed time determination, after which the time measurement unit is decoupled.

Berstis' abstract clearly discloses the applicant's claimed limitations. "A simple electronic horological device, termed a time cell, is presented with associated methods, systems, and computer program products. A time cell has an insulated, charge storage element that receives an electrostatic charge through its insulating medium, i.e. it is programmed. Over time, the charge storage element then loses the electrostatic charge through its insulating medium. Given the reduction of the electric potential of the programmed charge storage element at a substantially known discharge rate, and by observing the electric potential of the programmed charge storage element at a given point in time, an elapsed time period can be determined. Thus, the time cell is able to measure an elapsed time period without a continuous power source."

With respect to claim 2, Berstis clearly teaches decoupling the device from the external power supply. When the device is decoupled, the device must know that it is no longer coupled to the power supply, therefore a switching means must be inherent in the device.

With respect to claim 3, Berstis discloses in the abstract that the measuring means being used to determine an elapsed time. Specifically the "time cell" includes the charge storage element and given the known discharge rate of the electric potential of the charge storage device, the time cell is able to measure an elapsed time period without a continuous power source.

With respect to claim 4, Berstis discloses that the electronic entity is autonomous and that the electrical power supply is external to it. (see paragraph 0049).

With respect to claim 5, see paragraphs 0004, 0012, and 0033. Paragraph 0033 discloses that the smart card including the time cell is used to perform horological functions within commercial transactions, wherein multiple embodiments employ time cells in different ways to capture the multiple advantages that are provided by the unique horological characteristics of a time cell.

With respect to claim 6, Berstis discloses in paragraph 0044, that the measuring means includes a field-effect transistor whose gate is connected to a terminal of the capacitive component. Specially, a variety of programming mechanisms and programming times for charging the charge store element may be used, wherein the choice will be dependent on several factors, such as the size and composition of the insulating medium, the geometry of the charge storage element, etc. For example, if

the charge storage element is implemented as a floating gate within a floating gate field effect transistor (FGFET), then the charge process may be implemented via channel hot electron injection.

With respect to claim 17, as is explained above, the electronic entity is a smart card. Smart cards are microcircuit cards.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 7-11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Berstis in view of Baglee (5,049,958).

Berstis' teachings are discussed above. With respect to claims 8 and 20 Berstis discloses in paragraph 0063 a FGFET, wherein the gate is floating during the time that elapses between two connections or couplings to an external power supply on the occasion of two successive transaction. With respect to claim 9, Berstis teaches above that the transistor includes an insulative layer between the gate electrode and the substrate and the capacitive component also includes an insulative layer forming the dielectric space disposed between a plate and a substrate. With respect to claims 10 and 11, Berstis discusses in paragraph 0039 varying the thickness of the insulting layer in order to obtain the desired conduction of an electric charge. Claim 3 of Berstis discloses the thickness of the transistor's insulative layer. Berstis however fails to

specifically teach the FET to be a MOSFET and the capacitive component being a MOS technology capacitor whose dielectric space consists of silicon oxide.

With respect to claims 7-9, Baglee discloses in column 1, lines 17-20, that semiconductor memory devices of the dynamic read/write type traditionally are constructed using one-transistor cells with MOS storage capacitors which have silicon oxide dielectric.

In view of Baglee's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to use a MOS technology capacitor whose dielectric space consists of silicon oxide as is taught by Baglee, in the transactional electronic entity taught by Berstis. Baglee teaches that such MOS type storage capacitors are typically used in read/write memory devices (such as the device taught by Berstis). Therefore one would be motivated to use such a storage capacitor because of its known integrity, reliability, and functionality in a transactional electronic entity.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Berstis in view of Nakai (6,784,933).

Berstis' teachings are discussed above. Berstis however fails to specifically teach thickness of the insulative layer of the capacitive component being about 10 nanometers.

With respect to claim 12, Nakai discloses in column 5, lines 7-20, that the insulating medium (in the charge storage component) has a thickness of about 10 nm.

In view of Nakai's teachings, it would have been obvious to an artisan of ordinary skill in the art at the time the invention was made to use an insulative medium with a thickness of about 10 nm as is taught by Nakai in the transactional electronic entity taught by Berstis. Although Berstis does not teach the specific thickness of the insulating medium, one would be motivated to use a thickness of no more than 10 nm in order to keep the electronic entity to a minimum size.

***Allowable Subject Matter***

9. Claims 13-16 are objected to as being dependent upon a rejected base claim and also objected to above, but would be allowable if rewritten in independent form and overcoming the above objection, including all of the limitations of the base claim and any intervening claims.

The following is an examiner's for allowance: Although Berstis teaches a transactional electronic entity, which includes a capacitive component, a means for coupling the component to an electrical power supply to be charged, an a means for measuring the residual charge in the component, the above identified prior art of record, taken alone, or in combination with any other prior art, fails to teach or fairly suggest the specific features of claims 13-16 of the present claimed invention. Specifically, prior art fails to teach the electronic entity including at least two subsystems including at least two capacitive components having different leaks across their respective dielectric spaces and the electronic entity further including a means for processing measurements of the respective residual charges to extract from the measurements information substantially independent of heat input to the entity during the time elapsed between

two transactions. The claimed limitations discussed above are not disclosed in prior art and moreover, one of ordinary skill in the art would not have been motivated to come to the claimed invention.

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Kalogeropoulous (2004/0207363), Norton (2004/0099746), and Theobald (5,925,942).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Allyson N. Trail* whose telephone number is (571) 272-2406. The examiner can normally be reached between the hours of 7:30AM to 4:00PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee, can be reached on (571) 272-2398. The fax phone number for this Group is (571) 273-8300.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [**allyson.trail@uspto.gov**].

*All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published*

*in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.*

Allyson N. Trail
Patent Examiner
Art Unit 2876
August 9, 2007

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